REMARKS

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns a data controller that is couplable to a host and coupled to a storage medium, microprocessor, local storage and a buffer memory. The data controller generally comprises a command queuing engine that creates a plurality of threads of sequential commands that exist simultaneously while minimizing interrupts associated to the commands.

SUPPORT FOR SPECIFICATION AMENDMENT

Support for the amendment to the claims may be found, for example, on page 8 lines 19-25 of the specification, as originally filed. As such, no new matter has been added.

INTERVIEW SUMMARY

Applicant's representative, John Ignatowski, spoke with the Examiner, Ilwoo Park, on September 10, 2001 by telephone. The discussion was over the antecedent basis of the phrase "...creates a plurality of threads of sequential commands simultaneously...". The Examiner argued that "simultaneously" is limited to a single instance in time and thus the specification does not disclose creating multiple threads simultaneously. Applicants'

representative argued that "simultaneously" allows for a small but finite window of time in which the creation of multiple threads would be considered simultaneous. The Examiner and Applicants' representative agreed that the plurality of threads could exist simultaneously once created.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claim 1 under 35 U.S.C. §102(e) as being unpatentable over Olson et al., U.S. Patent No. 6,199,121, has been obviated by appropriate amendment and should be withdrawn. Claim 1 has been cancelled without prejudice or argument on the merits in the interest of placing the application in a condition for allowance.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1 and 5-11 under 35 U.S.C. §103(a) as being unpatentable over Garrett et al., U.S. Patent No. 6,049,842 in view of Bean et al., U.S. Patent 4,453,626 has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 2 and 12 under 35 U.S.C. §103(a) as being unpatentable over Ellis et al., U.S. Patent No. 6,029,226 in view of Krakirian, U.S. Patent No. 5,781,803 has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 13-15 under 35 U.S.C. §103(a) as being unpatentable over Ellis et al. in view of Krakirian and in further view of Bean et al. has been obviated by appropriate amendment and should be withdrawn.

Claims 1, 2, and 11-15 have been cancelled without prejudice or argument on the merits in the interest of placing the application in a condition for allowance.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claims 3 and 16-20 under 35 U.S.C. §112, first paragraph has been obviated by appropriate amendment and should be withdrawn.

The Examiner has previously agreed that the present invention discloses multiple threads coexisting, therefore no new issues have been created by the amendment to claim 3. There are no other outstanding rejections against claims 3 and 16-20. As such, the present application is in condition for allowance.

PRIOR ART OF RECORD

Applicant's representative respectfully disagrees with the Examiner's interpretation that Young, U.S. Patent No. 5,923,896 column 15 lines 26-28 teaches creating a plurality of threads of commands simultaneously. Young suggests in column 4 line 62 through column 5 line 4 that a chain structure is formed by

configuring a chain control field, a next block pointer, and a offset block pointer in each I/O command block in the chain. The offset block pointer may determine an alternative sequence of execution within the chain, but does not create a second chain. Furthermore, there is no motivation to combine Young with Ellis et al.. Ellis et al. focus on coalescing two write command descriptor blocks into a single disk command only if the logical block addresses match within a range. There is no motivation provided by Ellis et al. to incorporate the multiple-sequence chain taught by Young because the logical block addresses are not arranged as such in the storage device of Ellis et al..

While Applicants' representative doesn't necessarily agree with the interpretation of the references, the claims have been amended to further prosecution. Furthermore, Applicants' representative reserves the right to pursue broader claims in a continuation application.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 810-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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Dated: November 16, 2001

c/o Peter Scott
Intellectual Property Law Department
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Docket No.: 98-179 / 1496.00065

VERSION WITH MARKINGS TO SHOW CHANGES

3. (THREE TIMES AMENDED) A data controller, that is couplable to a host and coupled to a storage medium, microprocessor, local storage and a buffer memory, comprising a command queuing engine that creates a plurality of threads of sequential commands that exist simultaneously while minimizing interrupts associated to the commands.